Dr. MALI M. B.

Head, Department of E & TC

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OVERVIEW:

Qualifications: Ph.D.(VLSI), M. Tech., PG-CEP (IIT Bombay), GATE-95, BE, DIEE
Experience: Teaching -30 years Industry – ½years
Date of Joining STES: 08/01/2000
Skills and Proficiencies: Circuit design, Signal Integrity, Mixed Signal IC Design

SIGNIFICANT ACHIEVEMENTS:

- Member – Board of Studies (BoS), Savitribai Phule Pune University (SPPU).
- Special Invitee in BoS-SPPU for framing syllabi.
- Panel member in various committees of SPPU.
- Established Industry funded laboratories in liaison with Intel-FICE, Actel, Texas Instruments, ARM ST Microelectronics, e-Yantra, nVidia, Cypress & Xilinx.
- MoUs signed with Industries is 50+
- Establishment of an Incubation Centre with outcome of 8 Professional Incubatees-Beneficiaries.
- Examination work for several subjects at UG, PG & Ph.D. in University of Pune since more than 25 years.
- Certificates of Appreciation from Principal-Sinhgad College of Engg. for excellent performance.
- University first rank merit by Vice Chancellor in M. Tech.

AREA OF EXPERTISE /RESEARCH INTERESTS:

- Mixed Signal Chip Design

NUMBER OF STUDENTS GUIDED:

- Guiding 4 Ph.D. students, Ph.D. degree awarded to 2 students
- M.E. : 30+ students, UG : 80+ students

RESEARCH PULICATIONS:

Publication Summary:

Scopus/ SCI:14
International Journals: 43
Conference:94
h-index: 04
i10 index:0
No. of Books Authored: 2

No. of Books reviewed: 1

https://scholar.google.com/citations?hl=en&user=3bj9go8AAAAJ

Patents Granted/Published: Intelligent Vehicle Database and Access

FUNDED RESEARCH PROJECT:

- University of Pune funded research project on "VLSI Implementation of Low Drift, Low Power Band Gap Reference".
- **Consultancy Project** - Vehicle Tracking System for PSPL

RESEARCH WORK:

Research Work:

- VLSI Realization of CMOS Low Power High Speed Static Random Access Memory for Codebook

NOTABLE GUIDED PROJECTS:

- CMOS Transconductance Amplifier for High Speed Opamp
- Low Drift, Low Power CMOS Band Gap Reference (BGR)
- FPGA - Reconfigurable Motherboard
- Low Drop Out (LDO) Regulator
- PLL Digital Clock Manager
- SRAM Memory Design
- Reconfigurable CMOS IC Design

RESOURCE PERSON TO INDUSTRY/ACADEMIA:

- Resource person to more than 60 Institutes/Industries at State and National level

SUBJECTS TAUGHT:

- Analog CMOS Design
- Digital CMOS Design
- Reconfigurable Computing
- VLSI Design & Technology
- Electromagnetic Engg.

FDP/STTP/SDP/WORKSHOPS ORGANIZED AS A COORDINATOR:

- No. of FDP/SDP/STTP/Workshop/Seminars/ Summer Schools/Conferences organized: 20+

FDP/STTP/SDP ATTENDED:

- No. of FDP/SDP/STTP/Workshop/Seminars/ Summer Schools/Conferences attended: 50+

RESPONSIBILITIES HANDLED AT STES/SCOE/DEPT:

Society Level

- Senior Warden for Boys Hostels STES Vadgaon Campus.
- Incharge of Satellite Receiver on Vadgaon campus
- Faculty Interview Panel Member
- Incharge – Theme Events in Sinhgad Spring Fest

Institute Level (SCOE)

- NAAC Criterion Coordinator
- NBA Criterion Coordinator
- Member – Avishkar
- Organization of TIFAN
- Training to Newly Joined Faculty
- Grievances Committee Coordinator

Department Level (E&TC)

- Head – Department of E&TC Engg.

DECLARATION:

I hereby declare that all the above information furnished by me are true to the best of my knowledge.

Date: / / 2024 Signature