MRS. SNEHAL AJIT BHOSALE

EDUCATION :

Persuing PhD in E&TC Engg, G. H. Raisoni College of Engg & Management, Wagholi — 2014-15

Master Degree in Electronics, First Class **64.94%** July- 2011
(Specialization in Telecommunication)
Rajarambapu Institute of Technology, Islampur.

Bachelor in Electronics Engineering, First Class **63.14%** June- 2000
Karmaveer Bhaurao Patil College of Engineering. Satara.

H.S.C. **First Class with Distinction** **76.50%** June-1996
S.G.M. College, Karad Kolhapur Board

S.S.C. **First Class with Distinction** **88.57%** June-1994
Yashawant High School, Karad, Kolhapur Board

TEACHING EXPERIENCE (13 Years-11 Years Approved)

RMDSSOE Warje, Pune

Duration: 17th Dec'13 till date

RMDSSOE Warje, Pune (4 Years Approved)

Duration: 15th June'12 till date

Trinity College of Engg and Research, Pune (1 Year Approved)

Duration: 16th Aug'11 – 14th June'12 .

Sinhgad Institute of Technology, Lonavala (4 Years-2 Years Approved)

Duration: 26th June'07 -12th Aug'11

D.J.Sanghavi College of Engg, Vile Parle (W) (4 Years Approved)

Position : Lecturer (Information Technology Department)

Duration: Aug'03- June'07

INDUSTRIAL EXPERIENCE :(2.5 Yrs)

Training Executive in karRox Tech. Pvt. Ltd, Mumbai Apr'02-July'03

Network Design Engineer in Cisco System India Pvt Ltd, Bandra Kurla Complex, Mumbai Oct 01-Mar'02

Hardware/Network Engineer in Emtech AutomationPvt Ltd, Pune Mar'01-Sept'01

Microcontroller Programmer in GABSON DEVICES, Pune Jul' 00 – Jan' 01.

SUBJECTS TAUGHT (UG Level):

Basic Electronics Engg. Digital Logic Design, Communication Theory, Digital Communication, Data Communication, Digital Signal Processing, Computer Network, EDW Lab, Soft Skills, Network and Information Security, Foundation of Information Technology, Network Security, Principles of Communication, Computer Organization and Architecture, VLSI labs, Test and Measurement Techniques, ESED, Network Theory, EME.

SUBJECTS TAUGHT (PG Level):

Research Methodology, Embedded Signal Processing, Wireless Sensor Network.

PROJECT :

ME Level: FPGA based FM Demodulator for Wireless application

It is a FPGA based project in which FM demodulation is designed using VHDL. In this project received analog signal is converted into digital form using ADC . Digital down converter and Demodulation blocks are implemented using FPGA. For demodulation ARCTAN function is used which is implemented using CORDIC algorithms. Final signal is obtained by applying output of demodulator block to DAC.

HARDWARE SKILLS:

Completed a computer **Hardware course consisting of assembling, installations and troubleshooting and a course in networking in windows 2000 server** at NICE Computer Education Pune.

Completed a Networking course at Tate InfoTech Ltd ,Mumbai, consisting of **A+ CERTIFICATION ,COMPAQ M.C.S.E. (WIN 2000) ,SCO UNIX,CISCO and SUN SOLARIS** .(Duration 15th Sept 2001 to 14th Dec 2001).

Completed training on **Router and Switches Installation and configuration, VOIP implementaintion, Designing of WAN network** etc in **Computech Engineers, (Cisco's Premier Partner)Thane.**

LIFETIME MEMBERSHIP OF **ISTE** AND **IETE.**

CERTIFICATIONS:

CCNA certified in Dec 2001. **CSE (Security)** certified in Feb 2002.

WORK RELATED EXPERIENCE:

- Admission Committee member for 2 years in Dwarkadas J. Sanghvi COE, Mumbai.
- Co-coordinator for STTP on “Computer Aided Solutions for Engineering Application” in Dec’11 in D. J. Sanghvi COE, Mumbai.
- Time Table Committee member for 3 years in D.J. Sanghvi College of Engg, Mumbai.
- Student’s Association Co-ordinator in SIT Lonavala and Trinity COER.
- Co-ordinated a STTP on ‘Advanced VLSI and Embedded System’ in NOV-10.
- Prepared CD for DLD subject(SE- E&TC) at SAE, Kondhawa.DLD lectures available on U-tube.
- Working as T&P Co-ordinator for E&TC Dept, TCOER.
- Working as Head (In charge) in RMDSSOE since Dec’13.

NATIONAL CONFERENCES:

1. **‘**FPGA based Power Efficient Channelizer for Software Defined Radio’ at D.Y. Patil COE, Pimpari Chinchwad.
2. ‘Low Power System Design in modern VLSI’ at Amrutvahini COE, Sangamner.
3. ‘FPGA Based FM Demodulator For Wireless Application ’ at MAE Alandi.

INTERNATIONAL CONFERENCES:

1. ‘Comparitive study of Turbo codes using rate 1/3 constituent convolutional codes’ at SCTCOE, Trivendrum, Kerala.
2. ‘FPGA Based FM Radio Receiver For Software Radio.’ at Cummins COE, Pune.
3. ‘VLSI application in communication for implementation of FM Radio Receiver’ at Thakur COE, Mumbai.

INTERNATIONAL JOURNAL :

1. ‘FPGA based FM demodulator for wireless application’ titled paper is published in US based International Journal Computer Application (IJCA). *ICWET2010, Copyright 2010, ACM* 978-93-80747-70-1, February 26-27, 2010, Mumbai